In the claims:

Please amend the claims as indicated below.

1. (Twice Amended) An apparatus comprising:

a first drain bias network having an input suitable to couple to a FLASH cell;

a second drain bias network having an input suitable to couple to a FLASH cell; and

a sense amplifier having a first input, a second input, and an output;

an equalization circuit having a first node coupled to the input of the first drain bias network and having a second node coupled to the input of the second drain bias network and having a control signal to control operation of the equalization circuit[, wherein the equalization circuit is a single equalization transistor coupled between the first drain bias network and the second drain bias network.] by causing the equalization circuit to equalize the first input and the second input of the sense amplifier prior to changes induced by the first drain bias network and the second bias network.

2. (Amended) The apparatus of claim 1[further comprising:

a sense amplifier having a first input, a second input, and an output; and] wherein[:] the first drain bias network has an output coupled to the first input of the sense amplifier and the second drain bias network has an output coupled to the second input of the sense amplifier.

3. (Unchanged) The apparatus of claim 2 further comprising:

a reference FLASH cell coupled to the second drain bias network; and

a FLASH cell coupled to the first drain bias network.

4. (Unchanged) The apparatus of claim 3 wherein:

the reference FLASH cell coupled to the second drain bias network through a reference column select transistor and the FLASH cell selectively coupled to the first drain bias network through a column select transistor, the column select transistor controlled by a column select signal.

5. (Unchanged) The apparatus of claim 2 further comprising:

a FLASH cell coupled to the first drain bias network.

6. (Unchanged) The apparatus of claim 5 wherein:

the FLASH cell selectively coupled to the first drain bias network through a first column select transistor.

7. (Unchanged) The apparatus of claim 6 further comprising:

a reference FLASH cell coupled through a second column select transistor to the second drain bias network.

8. (Unchanged) The apparatus of claim 7 wherein:

the equalization circuit is a transistor having a first node coupled to the input of the first drain bias network and having a second node coupled to the input of the second drain bias network and having a control electrode coupled to a third node of the transistor, the control electrode to deliver the control signal.

9. (Unchanged) The apparatus of claim 4 wherein:

the equalization circuit is a transistor having a first node coupled to the input of the first drain bias network and having a second node coupled to the input of the second drain bias network and having a control electrode coupled to a third node of the transistor, the control electrode to deliver the control signal.

10. (Unchanged) The apparatus of claim 2 further comprising:

a reference FLASH cell coupled to the second drain bias network.

11. (Unchanged) The apparatus of claim 10 wherein:

the reference FLASH cell coupled to the second drain bias network through a reference column select transistor.

12. (Twice Amended) A method comprising:

equalizing a sense input and a reference input using a single equalizing transistor by causing the equalization transistor to equalize a first input and a second input of a sense amplifier prior to changes being induced by;

coupling the sense input to a FLASH cell to be sensed;

terminating equalization of the sense input and the reference input; and

measuring a sense voltage, the sense voltage corresponding to the sense input.

13. (Unchanged) The method of claim 12 further comprising:

selecting the FLASH cell.

14. (Unchanged) The method of claim 13 wherein:

coupling further includes loading the FLASH cell with a load.

15. (Unchanged) The method of claim 14 further comprising:

coupling the reference input to a reference FLASH cell, including loading the reference FLASH cell;

measuring a reference voltage, the reference voltage corresponding to the reference input; and

comparing the sense voltage and the reference voltage.

16. (Twice Amended) An apparatus comprising:

a first bias means for biasing a FLASH cell, the first bias means having an input and an output;

a second bias means for biasing a reference FLASH cell, the second bias means having an input and an output; and

a comparison means for comparing the output of the first bias means and the output of the second bias means;

a single equalizing transistor having a first node and a second node, the equalizing transistor coupled to the input of the first bias means and coupled to the input of the second bias means, the equalizing transistor to equalize a first input and a second input of the comparison means prior to changes induced by the first bias means and the second bias means.

17. (Amended) The apparatus of claim 16 further comprising:

[a comparison means for comparing the output of the first bias means and the output of the second bias means.]

a FLASH cell selectively coupled to the input of the first bias means.

18. (Amended) The apparatus of claim 17 further comprising:

[a FLASH cell selectively coupled to the input of the first bias means; and]

a reference FLASH cell coupled to the input of the second bias means.

19. (Unchanged) The apparatus of claim 18 wherein:

the input of the first bias means is disposed at a first node of the first bias means and the output of the first bias means is also disposed at the first node of the first bias means; and

the input of the second bias means is disposed at a first node of the second bias means and the output of the second bias means is also disposed at the first node of the second bias means.

20. (Twice Amended) A FLASH device comprising:

a FLASH cell array;

a control circuit block coupled to the FLASH cell array to control the FLASH cell array; and

a comparison circuit block coupled to the FLASH cell array and coupled to the control circuit block, the control circuit block to control the comparison circuit, the comparison circuit including:

a first drain bias network having an input suitable to couple to a FLASH cell,

a second drain bias network having an input suitable to couple to a FLASH cell, and

an equalization circuit having a first node coupled to the input of the first drain bias network and having a second node coupled to the input of the second drain bias network and having a control signal to control operation of the equalization circuit, [wherein the equalization circuit is a single equalizing transistor coupled between the first drain bias network and the second drain bias network] to cause the equalization circuit to equalize the first input and the second input of the comparison circuit prior to changes induced by the first drain bias network and the second bias network.

21. (Unchanged) The FLASH device of claim 20, further comprising:

a sense amplifier having a first input, a second input, and an output; and wherein:

the first drain bias network has an output coupled to the first input of the sense amplifier and the second drain bias network has an output coupled to the second input of the sense amplifier.

22. (Unchanged) The FLASH device of claim 21 further comprising:

a reference FLASH cell coupled through a column select transistor to the input of the second drain bias network; and wherein:

a selected FLASH cell of the FLASH cell array selectively coupled through a column select transistor to the input of the first drain bias network.

23. (Unchanged) The FLASH device of claim 22 further comprising:

a power supply circuit coupled to the control circuit block and to the FLASH cell array and to the comparison circuit block.

24. (Amended) An apparatus comprising:

a first bias network having an input suitable to couple to a persistent memory storage location;

a second bias network having an input suitable to couple to a persistent memory storage location; and

a sense amplifier having a first input, a second input, and an output;

an equalization circuit having a first node coupled to the input of the first bias network and having a second node coupled to the input of the second bias network and having a control signal to control operation of the equalization circuit[, wherein the equalization circuit is a single equalizing transistor coupled between the first drain bias network and the second drain bias network] by causing the equalization circuit to equalize the first input and the second input of the comparison circuit prior to changes induced by the first drain bias network and the second bias network.

25. (Amended) The apparatus of claim 24[further comprising:

a sense amplifier having a first input, a second input, and an output; and] wherein[:] the first bias network has an output coupled to the first input of the sense amplifier and the second bias network has an output coupled to the second input of the sense amplifier, the output of the first bias network having a relationship with the input of the first bias network, the output of the second bias network having a relationship with the input of the second bias network.

26. (Unchanged) The apparatus of claim 25 further comprising:

a reference persistent memory storage location coupled to the second bias network through a reference column select circuit and the persistent memory storage location selectively coupled to the first bias network through a column select circuit, the column select circuit controlled by a column select signal.

27. (Unchanged) An apparatus comprising:

a first drain bias network including:

a first transistor having a first node, a second node and a gate node, the first transistor coupled at its first node to a gate node of a second transistor, to a first node of a third transistor, and to a gate node of a fourth transistor, the first transistor coupled at its second node to ground, and the first transistor coupled at its gate node to a first node of an equalizing transistor and to a first node of the second transistor;

the second transistor having a second node, the second transistor coupled at its second node to a first node of the fourth transistor, to a first node of a fifth transistor, and to a second node of a sixth transistor;

the third transistor having a second node and a gate node, the third transistor coupled at its second node to a power supply, and the third transistor coupled at its gate node to the power supply;

the fourth transistor having a second node, the fourth transistor coupled at its second node to the power supply;

the fifth transistor having a second node and a gate node, the fifth transistor coupled at its second node to the power supply, and the fifth transistor

coupled at its gate node to the power supply; and

the sixth transistor having a gate node, the sixth transistor coupled at its gate node to a gate node of a sixth reference transistor, wherein the gate node of the sixth transistor is suitable to be coupled to a control signal;

a second drain bias network including:

a reference column select transistor having a first node, a second node and a gate node, the reference column select transistor coupled at its first node to a reference FLASH cell, the reference column select transistor coupled at its second node to a gate node of a first reference transistor, to a first node of a second reference transistor, and to a second node of the equalizing transistor;

the first reference transistor having a first node and a second node, the first reference transistor coupled at its first node to the gate node of the second reference transistor, to a first node of a third reference transistor, and to a gate node of a fourth reference transistor and the first reference transistor coupled at its second node to ground;

the second reference transistor having a second node, the second reference transistor coupled at its second node to a first node of the fourth reference transistor, to a first node of a fifth reference transistor, and to a second node of a sixth reference transistor;

the third reference transistor having a second node and a gate node, the third reference transistor coupled at its second node to the power supply, and the third reference transistor coupled at its gate node to the power supply;

the fourth reference transistor having a second node, the fourth reference

transistor coupled at its second node to the power supply;

the fifth reference transistor having a second node and a gate node, the fifth reference transistor coupled at its second node to the power supply, and the fifth reference transistor coupled at its gate node to the power supply; and

the sixth reference transistor having a first node, the sixth reference transistor coupled at its first node to the power supply; and

a sense amplifier including:

a first input coupled to the second node of the sixth transistor;

a second input coupled to the second node of the sixth reference transistor; and

an output.

28. (Unchanged) The apparatus of claim 27 further comprising:

a column select transistor having a first node, a second node and a gate node, the column select transistor suitable to be coupled at its first node to a FLASH cell, the column select transistor coupled at its second node to the gate node of the first transistor, and the column select transistor suitable to be coupled at its gate node to a column select signal.

29. (Unchanged) The apparatus of claim 28 further comprising:

a FLASH cell coupled to the first node of the column select transistor.

30. (Amended) An apparatus comprising:

a reference cell;

a kicker circuit;

a reference kicker circuit coupled to an output of the reference cell;

a first drain bias network coupled to the kicker circuit;

a second drain bias network coupled to the reference kicker circuit;

a sense amplifier with a first input to coupled to an output of the first drain bias network and the sense amplifier with a second input coupled to an output of the second drain bias network; and

an equalizing transistor, coupled between an input of the kicker circuit and an input of the reference kicker circuit, having a control signal to control operation of the equalization circuit by causing the equalization circuit to equalize the first input and the second input of the sense amplifier prior to changes induced by the first drain bias network and the second bias network.

31. (Unchanged) The apparatus of claim 30 further comprising:

the kicker circuit including:

a first transistor having a first node, a second node and a gate node, the first transistor coupled at its first node to a gate node of a second transistor, to a first node of a third transistor, and to a gate node of a fourth transistor, the first transistor coupled at its second node to ground, and the first transistor coupled at its gate node to a first node of the equalizing transistor and to a first node of the second transistor;

the second transistor having a second node, the second transistor coupled at its second node to the first node of the fourth transistor and to the first drain bias network;

the third transistor having a second node and a gate node, the third

transistor coupled at its second node to a power supply, and the third transistor coupled at its gate node to the power supply; and

the fourth transistor having a second node, the fourth transistor coupled at its second node to the power supply; and

the reference kicker circuit including:

a first reference transistor having a first node, a second node and a gate node, the first reference transistor coupled at its first node to a gate node of a second reference transistor, to a first node of a third reference transistor, and to a gate node of a fourth reference transistor, the first reference transistor coupled at its second node to ground, and the first reference transistor coupled at its gate node to a second node of the equalizing transistor and to a first node of the second reference transistor;

the second reference transistor having a second node, the second reference transistor coupled at its second node to a first node of the fourth reference transistor and to the second drain bias network;

the third reference transistor having a second node and a gate node, the third reference transistor coupled at its second node to the power supply, and the third reference transistor coupled at its gate node to the power supply;

the fourth reference transistor having a second node, the fourth reference transistor coupled at its second node to the power supply.

32. (Unchanged) The apparatus of claim 31 further comprising:

a column select transistor having a first node, a second node and a gate node, the column select transistor suitable to be coupled at its first node to a FLASH cell, the

column select transistor coupled at its second node to the gate node of the first transistor, and the column select transistor suitable to be coupled at its gate node to a column select signal.

33. (Unchanged) The apparatus of claim 32 further comprising:

a FLASH cell coupled to the first node of the column select transistor.